

Comparative Analysis of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverter using SPWM Technique

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ABSTRACT

This paper proposes comparison between symmetrical and asymmetrical Cascaded H-Bridge Multilevel Inverter (CMLI) using the multicarrier based SPWM Technique with induction motor as a load. Multilevel inverter have become more popular over the years in high power medium voltage application without the use of the transformer and with less disturbance & reduced harmonic distortion. In this paper three phase configuration of cascaded h-bridge multilevel inverter are studied. Here, carrier based sinusoidal pulse width modulation (SPWM) Technique is used as the modulation strategy. In this modulation strategy include the phase disposition technique (PD), phase opposition disposition technique (POD), and an alternative phase opposition disposition technique (APOD). All the study of the technique has been carried out the MATLAB/SIMULINK and evaluation of CMLI using SPWM technique in terms of THD.

Keywords

Cascaded H-bridge multilevel inverter (CMLI), Sinusoidal pulse width modulation (SPWM) technique, and Total harmonic distortion (THD).

1. INTRODUCTION

In recent era there is huge power requirement in industries and domestic applications. Generally simple inverter gives 2 or 3 level output voltage. Multilevel inverter gives more than 3 output voltage levels. As we know that multilevel inverter has becomes popular to fulfill power requirement, due to advantage of high power quality waveforms. The most attractive application of this technique are in the medium voltage (2.3-13.8 KV) and high power range (0.2-40 MW), and include motor drive, power distribution. Multilevel inverter include an array of power semiconductors and capacitor voltage sources with a single dc source or multiple dc source without capacitor voltage source, the output of which generate voltage with stepped waveform.

Owing to the recent popularity and immense industrial usage of multilevel inverters, a lot of research is going on in the field of multilevel inverter topologies. All these topologies have various applications along with their inherent limitations.

There are two methods of controlling multilevel inverters:

- PWM Control (allows variations in output voltage)
- Line Frequency Control (does not allow variation in output voltage)

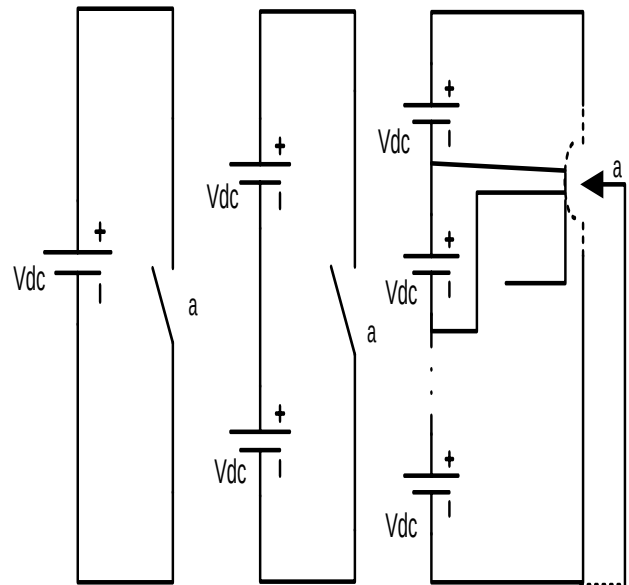


Fig 1: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n-levels

Multilevel inverters are basically 3 types:

- 1- Diode Clamped Multilevel Inverter
- 2- Flying Capacitor Multilevel Inverter
- 3- Cascaded H-Bridge Multilevel Inverter

We know that Diode clamped requires more no of diode and flying capacitor have balancing problem, and in these topologies structure have also complicated. Both are the not very used as compare to Cascaded H-Bridge Multilevel Inverter. As we know that the Cascaded H-bridge Multilevel Inverter having more no of advantages such as modular structure and therefore less components require as compare to other topologies. It is one of the topologies for drive application which requirements such as high power rating with reduced THD and switching losses. The Asymmetrical Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required.

IGBT is used as semiconductor switch for designing the inverter circuit.

2. SYMMETRICAL 5- LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

A relatively new power converter structure Cascaded H-bridge Multilevel Inverter many type separate source which is introduces here. First of all I want to introduce a simple H-bridge Multilevel Inverter. The AC terminal voltages of different level inverter are connected in series. The phase voltage is synthesized by the sum of inverter outputs.

Each and every single-phase full bridge inverter can give the 3 level outputs, $+V_{dc}$, 0 and $-V_{dc}$. In the fig.2 we seeing that give the output positive, negative and zero. When the switch S_{11}, S_{14} is ON then it gives the output positive, when the switch S_{13}, S_{12} ON then it gives the output negative and when the switch S_{11}, S_{13} or S_{12}, S_{14} ON then it gives the output zero. In symmetrical cascaded multilevel inverter, DC source of equal magnitude of voltage are used.

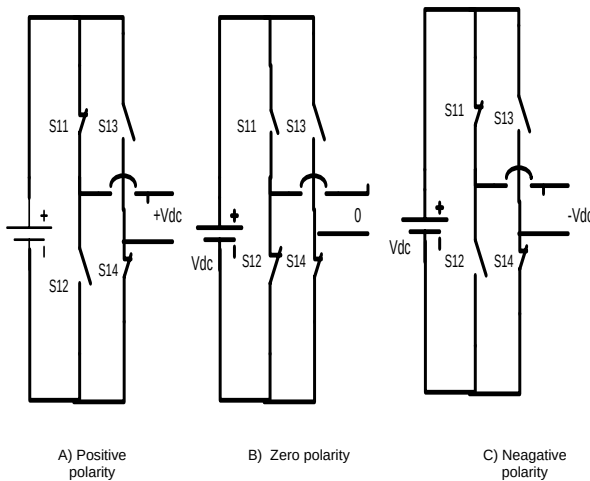


Fig 2: Output voltage polarities for the first H-Bridge cell

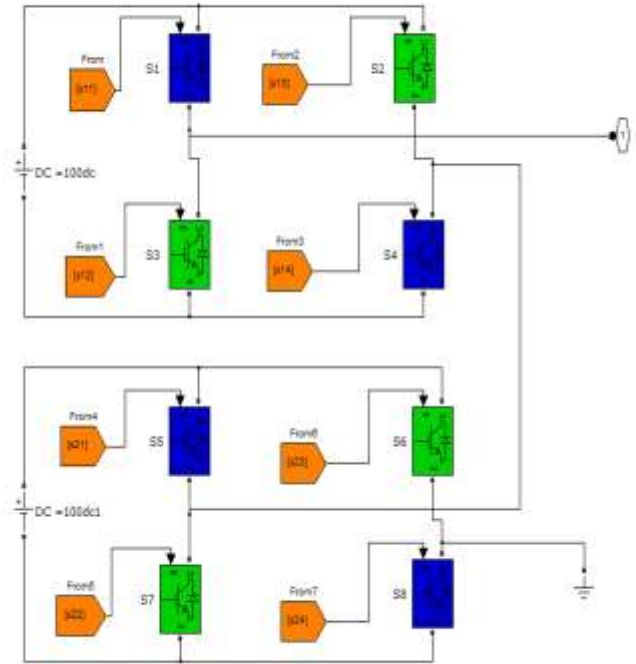


Fig 3: Topology of 5- level SCMLI

Table 1. Switching state of 5-level Symmetrical Cascaded H-Bridge Multilevel Inverter

S1	S2	S3	S4	S5	S6	S7	S8	Output
1	0	0	1	1	0	0	1	200Vdc
1	0	0	1	0	1	0	1	100Vdc
0	1	0	1	0	1	0	1	0
0	1	1	0	0	1	0	1	-100Vdc
0	1	1	0	0	1	1	0	-200Vdc

3. ASYMMETRICAL 7-LEVEL CASCADED MULTILEVEL INVERTER

In Asymmetrical Cascaded Multilevel Inverter, DC source of unequal magnitude of voltage are used. In case of Asymmetrical Cascaded Multilevel Inverter two unequal magnitudes DC source applied and the 8 power switches are used.

The basic modal circuit for 7-level Asymmetrical Cascaded Multilevel Inverter are shown in the fig.4 The Asymmetrical Cascaded 7 level Multilevel Inverter 2 DC source and 8 power switches and the magnitude of DC source 100V, and 200V respectively. The sources are connected to the two H-bridge units which are cascaded in signal phase. In an individual H-bridge gives the output a voltage is $+V_{dc}$, 0 and $-V_{dc}$. Hence the desired output voltage for the 7-level ACMLI are $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$.

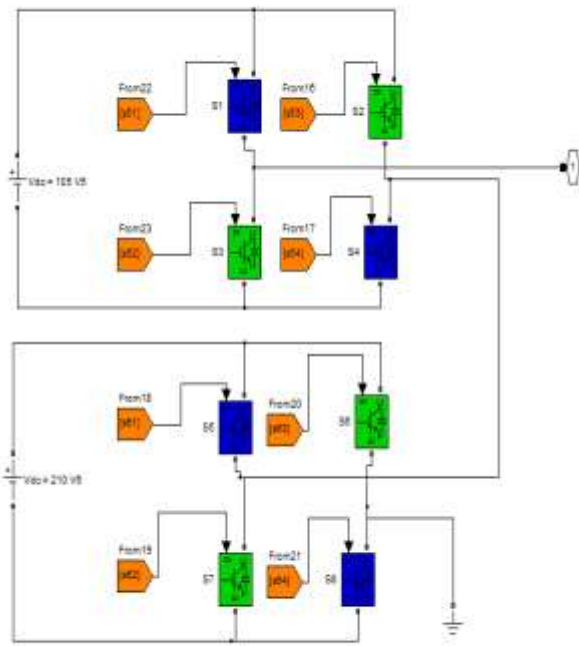


Fig. 4: Topology of 7- level ACMLI

Table2. Switching state of 7-level Asymmetrical Cascaded H-Bridge Multilevel Inverter

S11	S12	S13	S14	S21	S22	S23	S24	O/p V_{dc}
1	0	0	1	1	0	0	1	300
0	1	0	1	1	0	0	1	200
1	0	0	1	1	0	1	0	100
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	1	0	-100
0	1	0	1	0	1	1	0	-200
0	1	1	0	0	1	1	0	-300

4. MODULATION TECHNIQUE

Multilevel inverter has to synthesize a waveform by using the modulation technique. This modulation technique totally based on the comparison of a sinusoidal reference signal with carrier signal (same frequency) which is usually selected triangular pulses. The modulation schemes for multilevel inverter can be generally classified into the two categories: phase shifted and level shifted modulation. The reference signal has 50Hz frequency and the carrier waves have 2 kHz to 3 kHz are selected. Here we uses triangular generator for the purpose of carrier wave.

The frequency modulation index is given by:

$$m_f = V_{ref}/V_{car}$$

where V_{ref} is reference voltage and V_{car} is carrier voltage.

The amplitude modulation index is given by:

$$ma = A_m/A_{cr}(m-1)$$

where A_m amplitude of modulating signal, A_{cr} - amplitude of carrier signal, m- no. of levels.

There are basically three types of schemes of the level-shifted modulation

4.1 Phase Disposition Technique (PD)

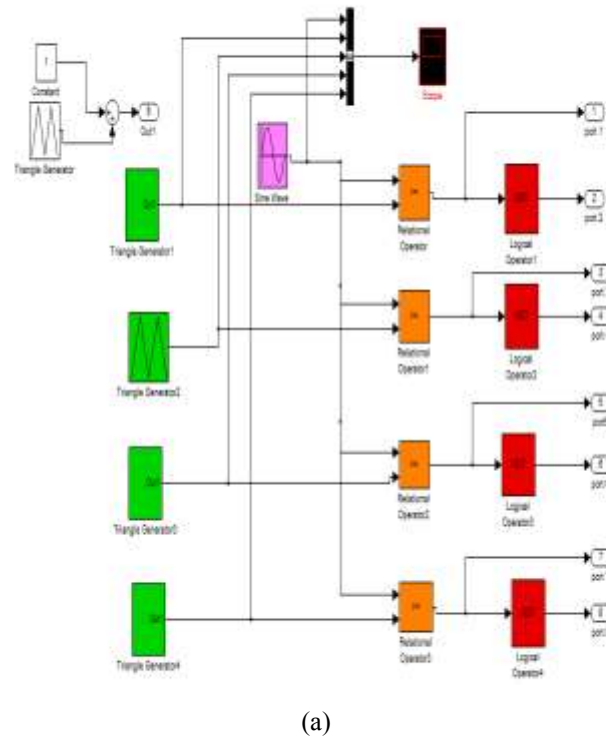
In this technique, all the vertical offset of carrier signals are adjacent to each other with same phase and the reference sine wave is placed in the middle of the carrier signals.

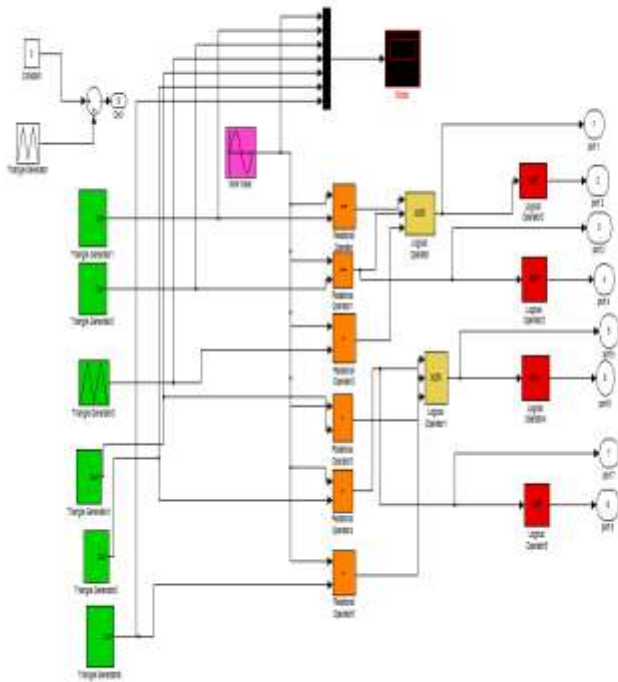
4.2 Phase Opposition Disposition technique (POD)

In this technique, they are divided equally into two groups according to the positive/negative levels. The two groups are opposite in phase with each other while keeping in phase within the groups and the reference sine wave is placed in the middle of the carriers.

4.3 Alternative Phase Opposition Disposition technique (APOD).

In the alternative phase opposition disposition technique (APOD), all the carrier are opposite in phase with each other and the reference sine wave is placed in the middle of the carriers.





(b)

Fig 5: Logic gates (a) 5- level (b) 7- level

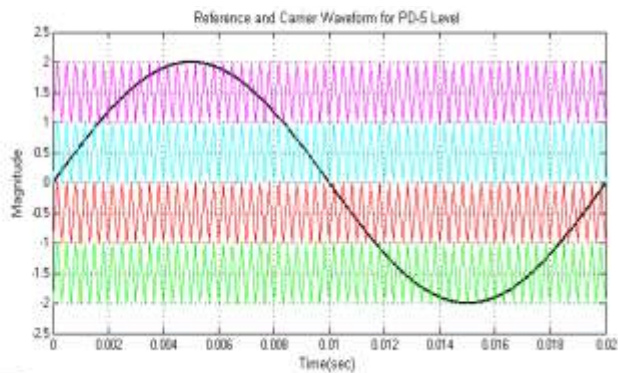


Fig 6: Reference and carrier waveform for PD 5- level

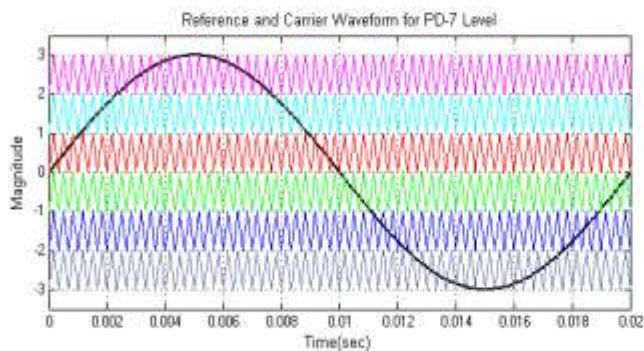


Fig 7: Reference and carrier waveform for PD 7- Level

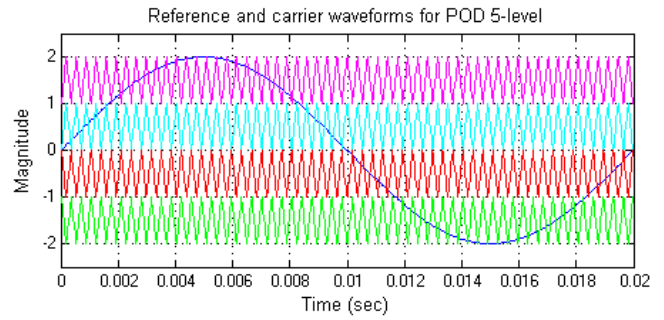
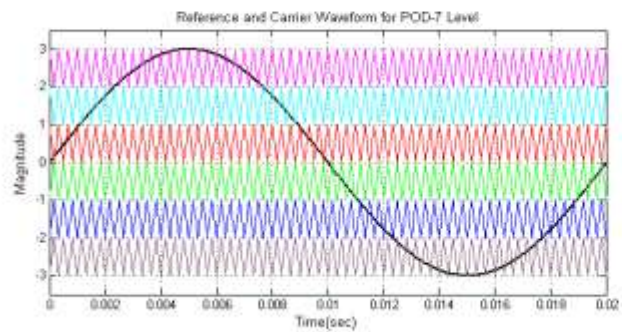


Fig.8 Reference and carrier waveforms for POD-5 level



Fig

9: Reference and carrier waveforms for POD-5 Level

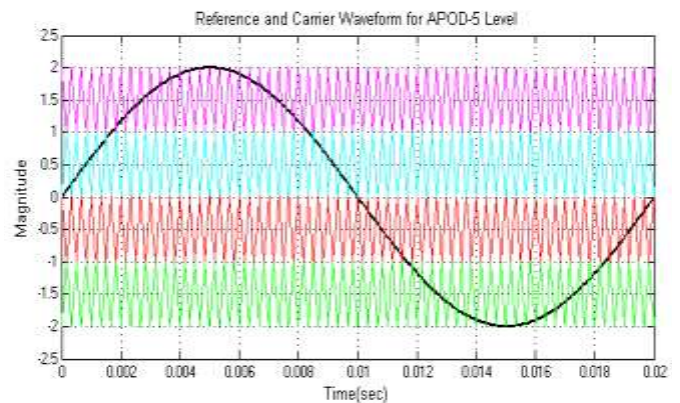


Fig 10: Reference and carrier waveforms for APD-5 level

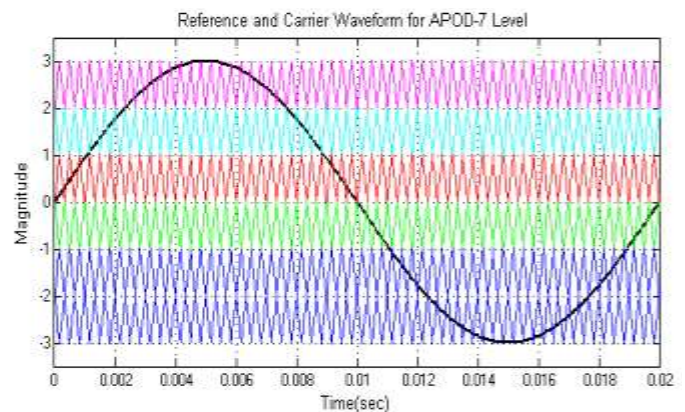


Fig 11: Reference and carrier waveforms for APD-7 Level

5. IMPLEMENTATION IN MATLAB

The complete results are observed in MATLAB/SIMULINK. The proposed converter synthesizes a three-phase multilevel output waveform from the switching modulation technique. MATLAB/SIMULINK is used to simulate 5 & 7-level CMLI fed induction motor drive, the complete simulative circuit for the 5 and 7 – level with an induction motor are shown in Fig 1. Parameters of three phase induction motor and the system is shown in Table. 3.

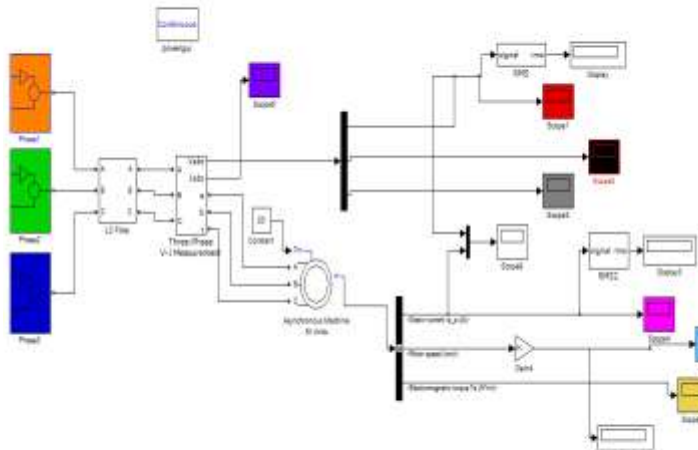


Fig.12 Simulation of 5 & 7-level inverter circuit with induction motor

Table 3. Ratings of three phase induction motor

Voltage (L-L) V	400v
Frequency f	50Hz
No. of poles p	4
Rated speed Nr	1440 rpm
Rated current I	7.825 Amp
Load torque Tl	20Nm
Nominal power of motor	10 HP (7.5KW)

6. SIMULATION RESULT

The performance analysis has been carried out using a three phase induction motor as a load with Cascaded H-Bridge Multilevel Inverter. The output voltage waveform of 5 and 7-level are shown in Fig 11 and Fig 12 respectively. The stator winding current, speed, torque of the induction motor and voltage and current waveform with filter are observed and are

shown in Fig 13, Fig 14, Fig 15 , Fig 16, Fig 17 and Fig 18 respectively.

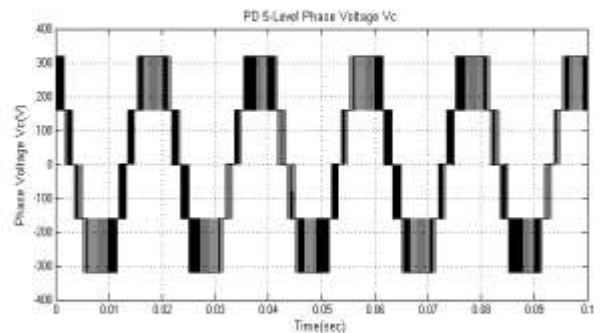
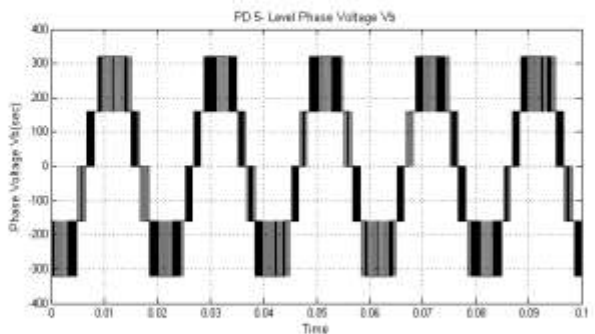
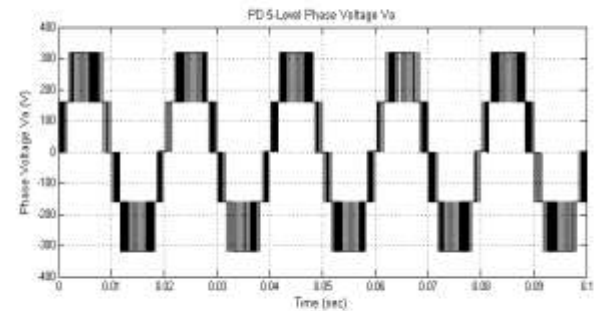
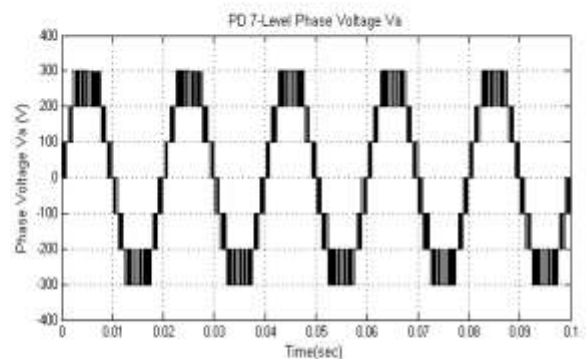


Fig 11: 5-level output voltage waveform



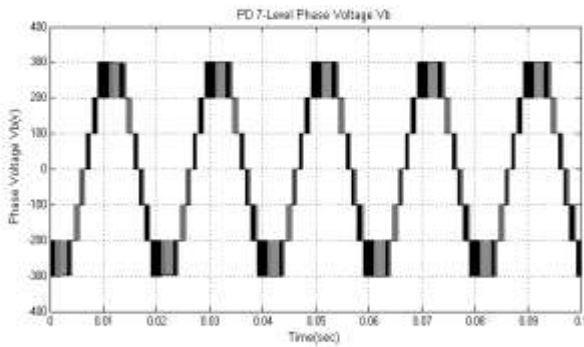


Fig 12: 5-level output voltage waveform

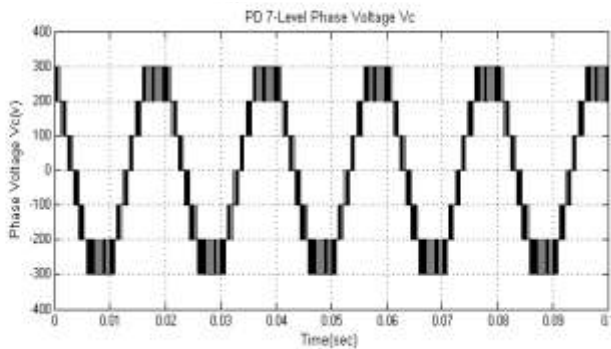


Fig 13: Three phase stator current for 5-level

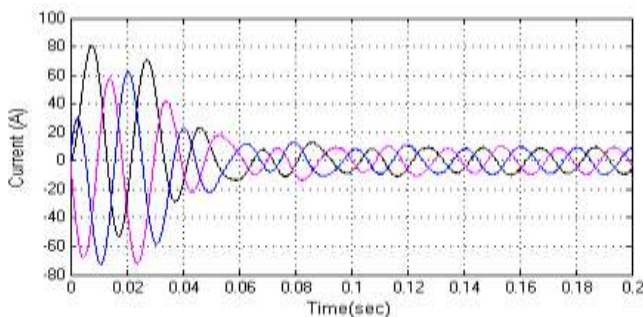


Fig 14: Three phase stator current for 7-level

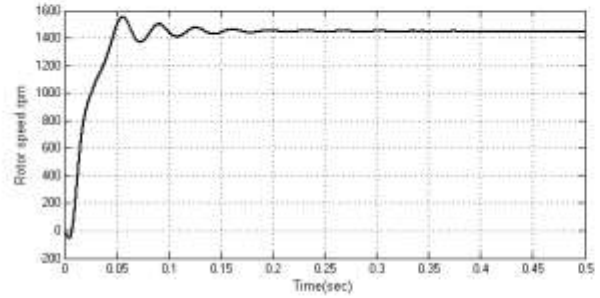


Fig 15: Rotor speed

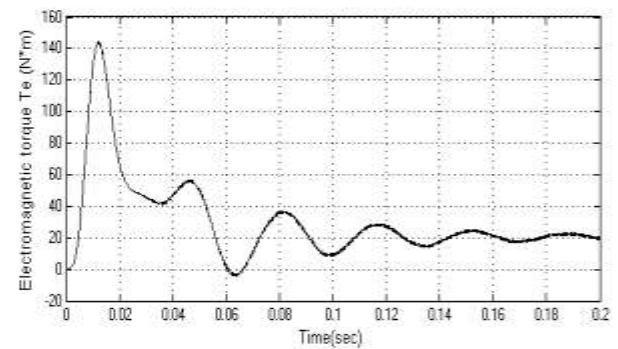


Fig 16: Electromagnetic torque (Nm)

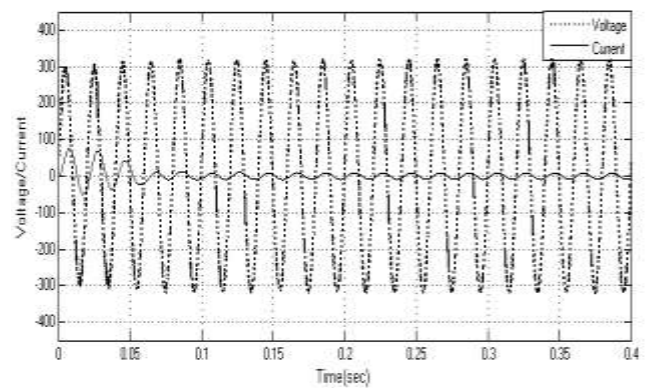


Fig 17: Voltage & Current of 5-level CMLI with filter

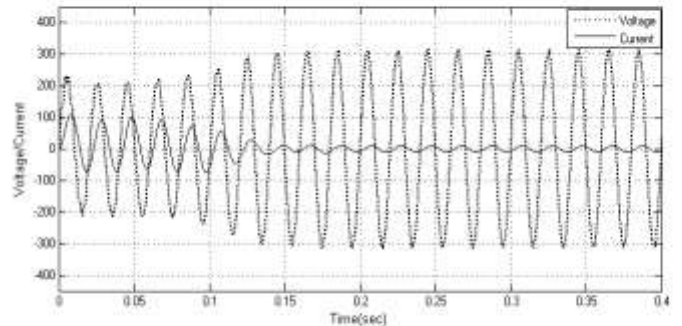


Fig. 18 Voltage & Current of 7-level CMLI with filter

The THD of the phase voltage V_a of both multilevel converter are compared for all the three SPWM technique i.e. PD, POD, APOD and are shown in Table. 4.

Table. 4 Comparison of both multilevel inverter in terms of THD %

Topologies	5-L SCMLI			7-L ACMLI		
SPWM	PD	POD	APOD	PD	POD	APOD
THD%	26.26%	26.31%	26%	17.84%	17.85%	17.62%
Topologies	5-L CMLI			7-L ACMLI		
SPWM	PD	POD	APOD	PD	POD	APOD
THD%	4.23%	6.37%	3.19%	2.11%	0.29%	0.25%
With filter						

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7. CONCLUION

This paper deals with a comparison of Symmetrical 5-level and Asymmetrical 7-level Cascaded H-Bridge multilevel inverter with induction motor as a load. It has been concluded that Asymmetrical CMLI, in general, is the best choice of MLI when it comes to component requirements, and less THD is observed for this topology. The THD of the phase voltage of both converter is studied under different SPWM modulation techniques such as PD, APOD, and POD and the less THD is observed for APOD technique. Multilevel inverter can be used instead of 2-level inverter to get lower THD and also to lower the switching losses for each device. By the help of these multilevel inverter we get the improved output voltage quality.

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