

Design of Efficient Circuits of D-Latch Using MOSFET, Sleep Transistor and Stacked Inverter Based on 32nm CMOS Technology

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ABSTRACT

In past few decades an unprecedented growth is experienced by electronics industry and the credit goes to the intelligent use integrated circuits in computation purpose, telecommunications and consumer electronics. When large number of transistors is used on a single chip, more power gets dissipated in the form of heat. Heat is a very important factor while designing any circuit. Heat is the main cause of driving low power design technologies. The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. D-latch ('data' latch) is the simplest in construction. Different designs of D-Latch have been designed using CMOS inverters, Transmission Gates, sleep transistors, Pass Transistors & GDI (Gate Diffusion Input) cell that can be operated at higher frequencies. All designs have been designed using 32nm UMC CMOS technology at 5GHz clock frequency. These designs are simulated in HSPICE tool for the successful function of the D-latch. It is being widely used in a complex optical communication system. Output changes when the clock signal is enabled. All the circuits have been designed in a 32 nm UMC CMOS technology to evaluate the efficiency of the proposed approach and experimental results show a correct behavior up to 5 GHz.

Keywords

Latch, D- Latch, CMOS, MOSFET, Transistor

1. INTRODUCTION

In past few decades developments in large scale integration resulted in millions of transistors placed on a single chip for execution of intricate circuitry. Maximum number of VLSI related applications such as DSP, image & video processing and microprocessors, widely uses logic gates and arithmetic

circuits. Operations such as AND, OR, addition, subtraction, and multiplication are usually used by these circuits. The building blocks of maximum digital circuits are logic gates, whereas in arithmetic circuits, 1-bit full adder cell is widely used. Thus, more constraints are being faced by the engineers such as: high speed, high throughput, small silicon area, and at the same time, low-power consumption. Therefore great interest was shown for designing of low-power, high performance adder cells. The two major limitations that are found during addition in DSP application from delay standpoint are latency and throughput.

In 1965 Gordon Moore (co- founder of Intel) predicted that as a result of continuous miniaturization, number of transistors in integrated circuit would double in every 18 months. In last 45 years compound annual growth rate is 53%. No other technology has grown so fast so long. Transistors became smaller, faster, cheaper and consume less power. "Figure 1" shows the increase in number of transistors during 1960 – 2000.

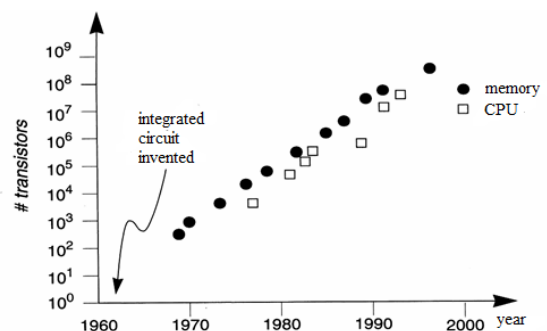


Fig 1: Number of transistors per year

2. LITRATURE REVIEW

The issue of clock signal generation and distribution in synchronous digital systems becomes ever more important as the performance (speed) demands on systems continue to rise dramatically, doubling approximately every three years. However, timing uncertainties have not remained proportional to frequency increases, and an increasingly large portion of the clock cycle has been spent on the clocking overheads. It has been predicted that traditional clocking techniques will cease to be useful in the 5 to 10 GHz range. New ideas are needed, for clock design and for the design of the systems they drive.

Static storage devices retain their logic states in the absence of clock signals, so long as the power supply is maintained. This type of approach to temporary storage is probably the one in widest use. And it is a mandatory one when data is to be saved once clock signals have been gated off, as in a piece of apparatus having a 'power-saving' mode. In dynamic storage device, logic states are represented by the electric charge on capacitive elements, elements which usually are the parasitic gate capacitances of the MOS transistors used in the storage elements.

The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. Because of its pervasiveness in such designs, it is perhaps the principal performance determinant, affecting the key characteristics of speed and power consumption. The two most common forms of this element are the latch and the flip-flop. Of these, the clocked D-latch ('data' latch) is the simplest in construction, the storage function being accomplished by a pair of cross-coupled inverters. The D-latch is such a device: it is a memory element having at least two inputs, namely a clock signal {CLK} and a data signal (D) and an output (Q) (and often its complement). The device is 'transparent' during one of the clock levels - the transparent phase - during which the output Q follows the input D. But when the clock level is complemented - to its isolation phase - the logic level present at D is frozen at Q, which remains in that state until CLK returns to its transparent phase. D-latches are categorized as being 'positive' or 'negative', depending upon the logic level of the transparent phase. Many papers are published in this area but We have designed D-Latch using different types of circuit components and techniques.

In 2010 [7], Martin Omana, Daniele Rossi and Cecilia Metra presented a paper entitled , "High-Performance Robust

Latches",IEEE. In this paper authors have proposed a new design of high performance robust latch which is insensitive to transient faults. They have also proposed a modified version of high performance latch which is used with clock gating. Cadence tool is used for simulation.

In 2011 [8], S. Lin, Y. B. Kim, and F. Lombardi presented a paper entitled, "Design and Performance Evaluation of Radiation Hardened Latches for Nanoscale CMOS",IEEE. In this paper authors have proposed three new hardened designs of CMOS latches based on Schmitt trigger. They have used 32nm CMOS library. Monte Carlo analysis is used for simulation.

In 2012 [9], Shankar Kumar Vijay, Sanjay Kumar Jaiswal, and Kumkum Verma presented a paper entitled, "Design and analysis of CMOS Inverter and D Latch MCML Inverter",International Journal of Advanced Trends in Computer Science and Engineering. In this paper authors have proposed a new design of D-Latch and implemented in MOS current mode logic. They have compared it with different values of power supply. They have designed the circuit using 180nm CMOS library simulated in Spice.

In 2013 [10], Saeideh Shirinzadeh, Rahebeh Niaraki Asli presented a paper entitled, "Design and performance evaluation of a low cost Full Protected CMOS Latch",IEEE. In this paper authors have proposed an efficient design of robust D-Latch which prevents transient pulses with no extra delay. They have designed the circuit using 45nm CMOS library.

In 2013 [11], Saeideh Shirinzadeh, Rahebeh Niaraki Asli presented a paper entitled, "High Efficiency Time Redundant Hardened Latch for Reliable Circuit Design",Springer. In this paper authors have proposed a high efficiency design of hardened D-Latch which uses undesired delay of Schmitt trigger circuit and a special feedback loop. They have designed the circuit using 45nm CMOS library.

In 2015 [12], V. P. Dhivyapriya, R. Nirmala and C. M. Kalaiselvi presented a paper entitled, "Analysis of Shift Registers Using Pulsed Latch",International Journal of Advanced Research in Computer Science and Software Engineering. In this paper authors have proposed design of CMOS based pulsed latch. They have designed the circuit using 32nm CMOS library and simulated in HSPICE simulation tool.

In 2017 [13], SumitraSingar, N. K. Joshi and P.K. Ghosh presented a paper entitled, "Novel Fault Resistant D-Latch for Low Power VLSI Design", International Journal of Engineering and Manufacturing Science. In this paper authors have proposed a novel design of robust fault resistant D-latch. They have designed the circuit using 45nm CMOS library and simulated in HSPICE simulation tool.

In 2017 [14], SumitraSingar, P.K. Ghosh, presented a paper entitled, "Unique Robust Fault Resistant D-Latch for Low Power Applications", IEEE. In this paper authors have proposed a novel design of robust fault resistant D-latch. They have designed the circuit for 1V power supply and 500 MHz clock frequency and simulated in HSPICE simulation tool.

3. METHODS

3.1 MOSFET

Today all integrated circuits are mainly based on MOSFET transistors. In earlier days mechanical switches were used by computers to calculate and solve Boolean functions. Now MOSFET transistors are used by the computers to develop and dominate our lives because of its fast, small and cool properties.

Digital integrated circuits use MOSFETs while analog circuits use BJTs. MOSFET [15] is a voltage controlled majority carrier device i.e. output current and voltage characteristics of MOSFET varies with the voltage on control terminal. This property describes the difference between the MOSFET and passive components like resistor, capacitor, inductor etc. One more difference is transistors have three terminals used for signal transmission while passive elements have two terminals. MOSFET is of two types: NMOS and PMOS.

3.2 CMOS

Today Complementary metal-oxide-semiconductor (CMOS) is being used in all integrated circuits, digital logic circuits, microprocessors, microcontrollers and others. It is also being used in several analog circuits such as CMOS sensors and others.

CMOS has two main characteristics viz. High noise immunity and low static power consumption. When transistors of CMOS devices switch between ON & OFF states, significant amount of power is drawn. CMOS circuits produce less heat as waste in comparison to Logic circuits like transistor-transistor logic (TTL) or NMOS logic. A chip can contain high density of logic circuits made by CMOS devices. Today this technology is being used in all VLSI chips.

3.3 SLEEP TRANSISTOR

State-destructive techniques cut off the transistors (PMOS pull-up or NMOS pull-down or sometimes both) networks from supply voltage or ground by using sleep transistors [17]. These types of methods are also known as gated-GND and gated V_{dd} (Also note that a gated clock is normally used for dynamic power reduction). Mutoh et al. have proposed a technique called as Multi-Threshold Voltage CMOS (MTCMOS), it adds high- V_{th} sleep transistors between PMOS pull-up networks and V_{dd} and between NMOS pull-down networks and GND. The sleep transistors are switched off while the logic circuits are not in usage. By using sleep transistors the logic networks are isolated; the sleep transistor method dramatically lessens leakage or static power during sleep mode. Though, the additional sleep transistors take more area and produce more delay. Furthermore, the PMOS pull-up and NMOS pull-down networks have floating values and therefore it loses state during sleep mode. These floating values considerably influences the energy and wakeup time of the sleep transistor technique due to the necessity to recharge transistors which have lost their state during sleep.

3.4 LATCH

The one-bit digital storage element plays a fundamental role in digital signal processing circuitry. Because of its pervasiveness in such designs, it is perhaps the principal performance determinant, affecting the key characteristics of speed and power consumption. The two most common forms of this element are the latch and the flip-flop. Of these, the clocked D-latch ('data' latch) is the simplest in construction, the storage function being accomplished by a pair of cross-coupled inverters. Of the various flip-flop structures available (J-K, S-R etc.), the one used most frequently in synchronous digital circuits is the DFF ('data' flip-flop), by reason of its simplicity and resulting high speed of operation and also the fact that it is very easily implemented using contemporary IC fabrication technologies.

3.4.1 D-Latch

The D-latch whose waveforms are shown in "Figure 2" is such a device [2]: it is a memory element having at least two inputs, namely a clock signal (CLK) and a data signal (D) and an output (Q) (and often its complement). The device is 'transparent' during one of the clock levels the transparent phase during which the output Q follows the input D. But when the clock level is complemented to its isolation phase

the logic level present at D is frozen at Q, which remains in that state until CLK returns to its transparent phase. D-latches are categorized as being 'positive' or 'negative', depending upon the logic level of the transparent phase.

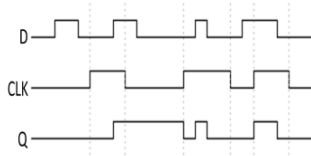


Fig.2: D Latch waveforms

3.4.2 Master-Slave Latch

Transparency in latches can be responsible for instability, glitches and race conditions. These problems can be done away with by using an arrangement of two latches which are clocked successively with two non-overlapping clock phases [2, 3]. The first latch serves as a 'master' which receives data input and passes it on to a 'slave' latch, as in "Figure 3". The non-overlapping nature of the CLK phases ensures that there is no transparency between the input and the output; most often the other phase of the clock is achieved by locally inverting the main clock.

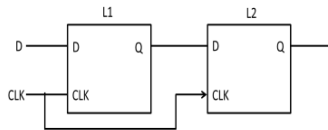


Fig. 3: Master-Slave latch

3.4.3 Static D-Latch

The structure of static D-Latch is shown in "Figure 4". It is based on a Set-Reset (SR) latch made of cross-coupled NOR gates [1-3]. When CLK is high the AND gates are enabled and Q follows changes in D (transparent mode). But when CLK goes low, the current state of D is frozen at the Q output, which is then not affected by further changes in D. An inverter between the S and R latch inputs prevents disallowed states. This latch uses a single clock, but as one can see, the device count is still high. The circuit complexity and number of propagation delays makes this structure unsuitable for high speed applications.

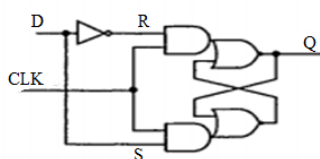


Fig. 4: Static D-Latch

3.4.4 Dynamic D-Latch

A completely different means of realizing a latch involves representation of data as the charge (voltage) of a capacitor. The capacitor is used to store the input value at high CLK phase just before CLK goes low and transmission gate turns off. The capacitor is not explicitly included, but is the parasitic input capacitance of the inverter and of the transmission gate.

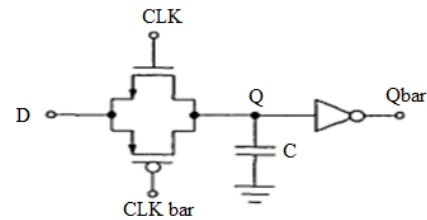


Fig. 5: Dynamic D-Latch

The dynamic latch must be refreshed periodically; otherwise its value can be corrupted due to the leakage currents of the transmission gate junction. This imposes minimum frequency on the clock signal. For this reason, dynamic latches are used only when it is known a priori that they will always be clocked.

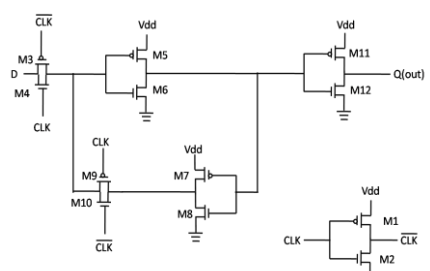
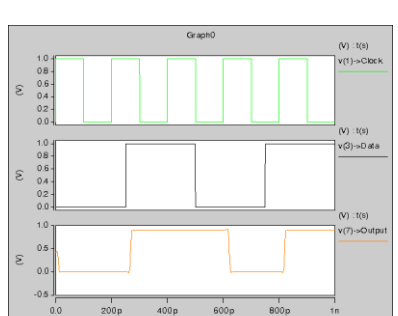
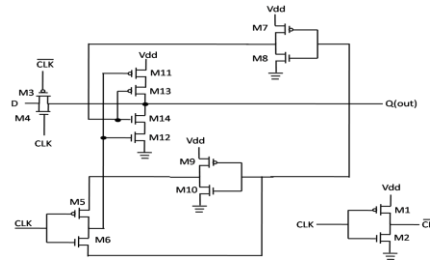
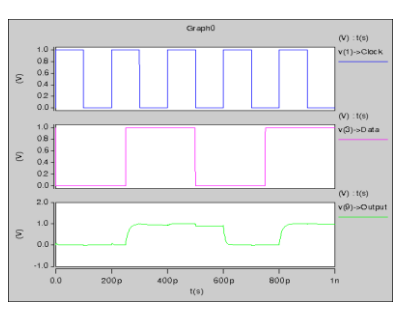
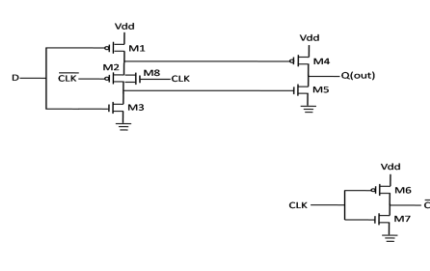
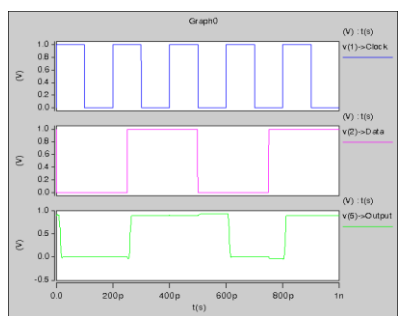
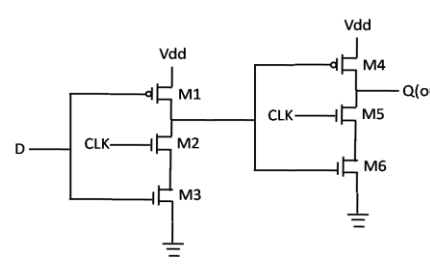
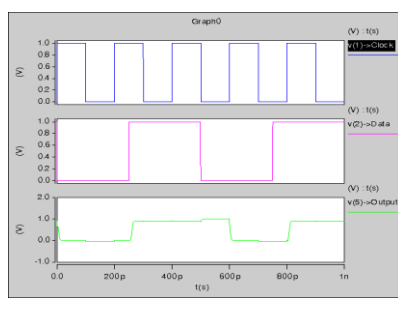
4. PROPOSED METHODOLOGY

In this section have defined proposed work which we have performed in HSPICE simulation tool. In this work we have designed some efficient circuits of D-Latch using MOSFET which consumes less average power. All circuits are designed using 32nm CMOS technology at 5 GHz. Power supply is 0.9V. ("Table 1") mentions the initial parameters that are taken to make the pulse for inputs D and Clock. In ("Table 2") we have 6 designs of D-latch with their design, dimensions, and output.

Table 1: Initial Parameters

$V_{dd} = 0.9V$, $L = 32nm$			
Input	Delay(sec)	Rise Time (sec)	Fall Time(sec)
D & Clock	0.025F	0.3P	0.3P

Table 2: Different D-latch designs with MOSFET dimensions and output

Sr. No.	D- latch design	MOSFET dimensions	Output																														
1.	 It is the simplest method to demonstrate the working of D-Latch.	<table><tr><th>MOSFET</th><th>W/L ratio</th></tr><tr><td>M1</td><td>0.438</td></tr><tr><td>M2</td><td>0.469</td></tr><tr><td>M3</td><td>0.406</td></tr><tr><td>M4</td><td>0.406</td></tr><tr><td>M5</td><td>0.406</td></tr><tr><td>M6</td><td>0.875</td></tr><tr><td>M7</td><td>0.375</td></tr><tr><td>M8</td><td>0.344</td></tr><tr><td>M9</td><td>0.344</td></tr><tr><td>M10</td><td>0.406</td></tr><tr><td>M11</td><td>0.344</td></tr><tr><td>M12</td><td>0.406</td></tr></table>	MOSFET	W/L ratio	M1	0.438	M2	0.469	M3	0.406	M4	0.406	M5	0.406	M6	0.875	M7	0.375	M8	0.344	M9	0.344	M10	0.406	M11	0.344	M12	0.406					
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2.	 When clock (CLK) is high, M3, M4 conducts and input D passes to the output.	<table><tr><th>MOSFET</th><th>W/L ratio</th></tr><tr><td>M1</td><td>0.563</td></tr><tr><td>M2</td><td>1.094</td></tr><tr><td>M3</td><td>0.563</td></tr><tr><td>M4</td><td>1.094</td></tr><tr><td>M5</td><td>0.563</td></tr><tr><td>M6</td><td>0.344</td></tr><tr><td>M7</td><td>0.469</td></tr><tr><td>M8</td><td>0.875</td></tr><tr><td>M9</td><td>0.625</td></tr><tr><td>M10</td><td>1</td></tr><tr><td>M11</td><td>0.344</td></tr><tr><td>M12</td><td>0.375</td></tr><tr><td>M13</td><td>0.438</td></tr><tr><td>M14</td><td>0.438</td></tr></table>	MOSFET	W/L ratio	M1	0.563	M2	1.094	M3	0.563	M4	1.094	M5	0.563	M6	0.344	M7	0.469	M8	0.875	M9	0.625	M10	1	M11	0.344	M12	0.375	M13	0.438	M14	0.438	
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3.	 In this design when clock is high M2 and M8 conducts and creates short circuit between M1 and M3.	<table><tr><th>MOSFET</th><th>W/L ratio</th></tr><tr><td>M1</td><td>1.094</td></tr><tr><td>M2</td><td>2.031</td></tr><tr><td>M3</td><td>1.563</td></tr><tr><td>M4</td><td>2.031</td></tr><tr><td>M5</td><td>1.25</td></tr><tr><td>M6</td><td>0.375</td></tr><tr><td>M7</td><td>0.469</td></tr><tr><td>M8</td><td>0.938</td></tr></table>	MOSFET	W/L ratio	M1	1.094	M2	2.031	M3	1.563	M4	2.031	M5	1.25	M6	0.375	M7	0.469	M8	0.938													
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5.

In this design when clock is high M5, M6 conduct and passes input data to the output terminal.

MOSFET	W/L ratio
M1	0.563
M2	0.406
M3	0.375
M4	0.375
M5	0.438
M6	0.375

6.

In this design when clock is high M4, M5 gets ON. If D = '0', logic '1' passes through M3, M5 then gets inverted by M7 & M8 and we get the same data at the output terminal.

MOSFET	W/L ratio
M1	0.563
M2	0.406
M3	0.375
M4	0.375
M5	0.438
M6	0.375
M7	0.465
M8	0.563
M9	0.375
M10	0.247
M11	0.543
M12	0.375

5. RESULT ANALYSIS

These results show improvement in PDP and power consumption compared to some existing latches. Comparison between different D-Latch designs is represented in detail as shown in “Table 3”.

Table 3: Comparison between designs of D-Latch

Design No.	No. of Transistors	Average Power (μW)	Delay Time (ps)	PDP (fJ)
1	12	0.38	319.5	0.12
2	14	0.35	306.04	0.11
3	8	0.13	12.44	0.002
4	6	0.07	8.06	0.006
5	6	0.16	2.44	0.004
6	12	0.26	21.5	0.005
Ref [14]	14	1.05	38.1	0.04

D-latch configurations can be designed more efficiently with less power supply, less delay, less area and advanced CMOS technologies. By optimizing transistors' sizes, advanced technology preferred complex circuits can be designed. Graphical representation of these results is shown below.

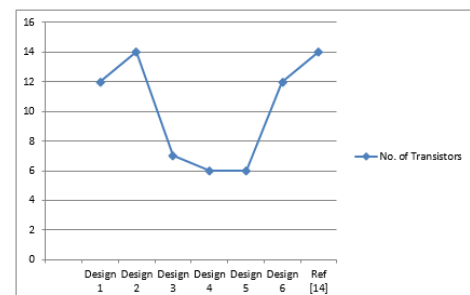


Fig. 6. Designs versus number of transistors

6. CONCLUSION AND FUTURE WORK

In this paper we proposed different designs of low power full protected CMOS latch. HSPICE simulations using 32nm UMC CMOS technology have been performed for all the configurations of D-latch. The results demonstrate the efficient working of latch with optimized average power, time delay, power delay product and number of transistors. The best optimized configuration of D-latch is “Design based on sleep transistor” which consumes 0.26 μW average power, gives 21.5 ps time delay. It has power delay product (PDP) of 0.005 fJ which is very much beneficial for high speed communication circuits. In future D-latch configurations can be designed more efficiently with less power supply, less delay, less area and advanced CMOS technologies. By optimizing transistors' sizes, advanced technology preferred complex circuits can be designed.

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