

Switching and Multicast Schemes in Asynchronous Transfer Mode Networks

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ABSTRACT

The purpose of this paper is to provide an overview of the ATM switching technology and to describe various multicast schemes in ATM Networks. One of the most promising solutions of ATM switches is based on the shared-memory principle. A shared-memory ATM switch provides sharing of memory space among its switches ports and superior cell loss rate performance compared to input-buffer-based and output-buffer-based ATM under conditions of identical memory size. We studied various multicast schemes, which are presented in this paper.

Key Words: ATM Switch, buffer allocation, multicasting, queue length threshold, shared memory switch.

1. INTRODUCTION

The telecommunications industry is rapidly becoming a high bandwidth and high speed network environment due to fast growing market demands for multimedia applications. New multimedia based applications (such as data, voice, video and image) require greater bandwidth with capability of handling multiservice traffic on the same network. One technology known as asynchronous transfer mode (ATM) was developed and is continually being further enhanced to meet this demand.

ATM is a high speed, packet switching network technology capable of supporting many classes of traffic. It incorporates the advantage of fiber optic techniques to transport a wide range of traffic types such as voice, video, image and various data traffic.

ATM is a standard being developed by 2 major organizations: the ATM Forum and the ITU-T. The ATM standards define guidelines needed to support cell-based voice, data, video, and multimedia communication in a public network under Broadband ISDN. Although ATM standards are very well defined, there is one area that is not included in the overall standard. It is the area of ATM switching. By default, ATM switch vendors use a wide variety of techniques to build their switches based on their own research and development efforts. Therefore, this paper will provide the reader with ATM basics overview in addition to a general description of the major components of an ATM switch and various switch design techniques being implemented by ATM switch vendors.

2. ATM SWITCHING FUNCTIONS

As described earlier in previous sections, user traffic information is routed through the network via virtual paths or channels. Therefore, one key function of an

ATM switch is its ability to buffer cells and quickly relay them without cell loss. However, ATM switches not only relay cells but must also perform control and management functions in

order to support both asynchronous and synchronous traffic as well as connectionless and connection-oriented traffic.

An ATM switch contains a set of input and output ports, which are utilized to interconnect to users, other switches, and other network elements. It also has interfaces

to exchange control and management information with special purpose networks (i.e., network management systems).

According to ATM standards, the switching function of ATM switches are categorized into 3 planes based on the Broadband ISDN model: User plane (U-plane), Control plane (C-plane), and Management plane (M-plane). The User plane relay user information cells from input ports to appropriate output ports by processing cell headers. It is useful to note that in the User plane, cell payloads are carried transparently through the network. Therefore, this cell relay function can be divided into 3 major blocks: the input module at the input port, the cell switch matrix that performs the routing function, and the output modules at the output ports.

The Control plane deals with call establishment and release of virtual path/virtual channel connections. Information in control cells payload is not transparent to the network because it contains signaling information required for setting-up connections.

The Management plane provides management functions to ensure correct and efficient network operation. The management function can further be divided as follows:

- ☐ Fault management
- ☐ Performance management
- ☐ Configuration management
- ☐ Security management
- ☐ Accounting management
- ☐ Traffic management

3. MULTICASTING SCHEMES

3.1 UNICASTING AND BROADCASTING

Unicasting means sending a message from a single source to a single destination. Whereas in broadcasting a message is sent to all the destinations like in the television, the signals are broadcasted to all the destinations through the satellites.

3.2 Multicasting

Multicast can be simply defined as the ability to send one message to one or more in a single operation. This is different than using replicated unicast which sends messages from one node to a group of nodes by sending to each node individually. This will incur one operation for each destination node and is non-atomic. A 1:N multicast allows one source to reach N

destinations. An M:N multicast allows M sources to reach N destinations.

3.3 Why Multicasting ?

Many envisioned applications in asynchronous transfer mode (ATM) networks are multicast in nature and are expected to generate a significant portion of the total traffic. Examples of such applications are broadcast video-conferencing, multiparty telephony and work group applications. The ability to support multicast traffic is therefore a basic functionality that needs to be implemented in ATM switches. Mechanisms have to be provided in the switches to replicate cells arriving at an incoming

multicast virtual connection (VC) and deliver them to multiple outgoing legs of that connection.

4.REQUIREMENTS FOR ATM MULTICAST

ATM imposes specific requirements [11] that must be considered for the design of the multicast services. The short, fixed length of the ATM cell requires an adaptation layer at the end points to transfer complete message and guarantee that cells from different sources are not interleaved by intermediate switches. The overhead of call setup and tear-down for the connection based ATM protocol require an efficient mechanism for adding and removing users to a multicast group. The limited size of the VPI/VCI field prevents the use of source-based routing, as used by the existing IP multicast routing programs

	A		B		C		D	
Timing	Real Time	None	Real Time	None	Real Time	None	Real Time	None
Bit rate	Constant		Variable		Constant		Variable	
Mode	Connection Oriented				Connectionless			

Table 1. Multicast Application Characteristics scheme.

gives an indication of the requirements of those application types that would require multicasting protocols. Connection oriented protocols can incur a high overhead when setting up and destroying links, therefore connectionless links are preferable. Some applications that require multicasting such as audio would prefer a constant bit rate where as video is less susceptible to the jitters. This is due to a human's high sensitivity to audio jitters. It can then be taken from the Fig.[1] that class D services are along the lines needed to implement multicast on an ATM network. More advanced details could be studied in [15-22].

5.MULTICASTING SCHEMES FOR SHARED MEMORY SWITCH

Various ways of supporting multicast operation with shared-memory architecture can be categorized under two different classes :

□ Replication-at-Receiving (RAR) or copying Network

□ Replication-at-Sending (RAS)

A brief description of each of the multicast classes is given below.

5.1 RAR schemes

In RAR scheme, a multicast cell arriving at the switch and destined to m destinations is first copied m times Fig.[1]. A copy of the cell is linked to each output queue to which the multicast cell is destined. All copies are stored in the buffer then each copy is served independently.

The RAR scheme has been used in several existing shared memory switches because it is relatively simple to implement [3]. In fact, once a cell has been replicated each copy of the cell can be treated in the same way as a unicast cell. Consequently, both the control and the structure of the linked lists are basically the same as those used in a unicast switch.

MWMMR Multicast Scheme

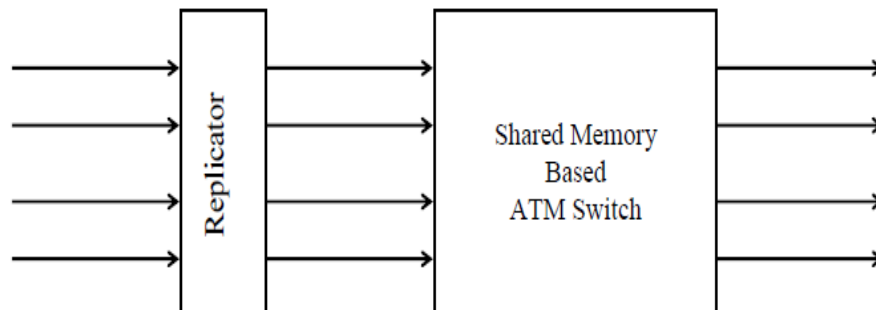


Fig.[1] Shared Memory : Multicasting with copying n/w

5.2 RAS scheme In RAS scheme the multicast cell is not replicated before storage in shared buffer, only single instance

of cell is stored in the buffer. Cell is replicated at the output port. This is shown in Fig.[2].

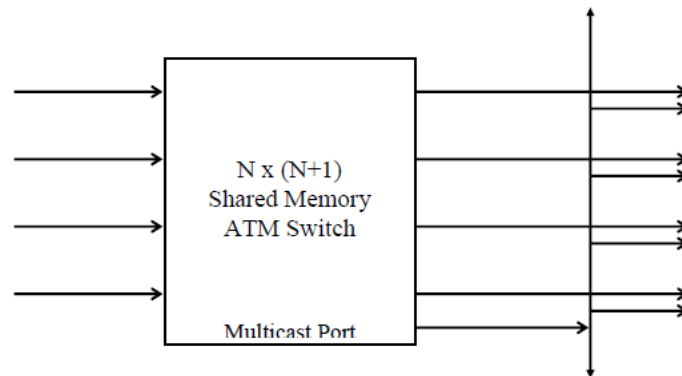


Fig. [2] SWSR Multicast Support employing a Fanout bus

5.3 Multiple Write Multiple Read (MWMR)

This is a straightforward solution to providing multicast support. The MWMR scheme applies to all those multicast schemes where an incoming multicast cell is replicated first, and then its multiple copies are used to write into and read out of the shared memory space for switching purpose. A multicast cell is replicated for all its multicast connections and switched to a predestined group of output ports with the help of a point-to-point routing network before being written to the shared memory space.

From a shared memory point of view, a multicast cell is replicated into multiple copies and stored in shared memory (multiple write); then multiple copies are eventually read out of the shared memory (multiple read) for their respective output port.

Advantages of MWMR scheme:

In the MWMR scheme, multicast cells after replication are treated the same as the unicast cells. This scheme is a fair scheme in the sense that copies of a multicast cell destined to a loaded output are more likely to be dropped and an idle output port would always get its cell if the copies are present in the memory.

Disadvantages of MWMR:

The biggest disadvantage of this approach is that for an effective load, the number of replicated cells input to the shared memory switch could be of $O(N_2)$. As in the worst case, N cells might get replicated to at most N_2 cells and only at most N cells could be transmitted in a given switch cycle. This would result in storing $O(N_2)$ cells in each switch cycle, and for a finite memory space it would result in an considerable cell loss for a given effective load.

Furthermore replication of multicast cells would require $O(N_2)$ ATM cells to be written to the shared memory space in a given switch cycle. This scheme obviously becomes limited by the memory cycle time as the degree of fanout increases in a large shared memory based ATM switching system.

5.4 Single Write Single Read (SWSR)

In this scheme, multicast cells form a separate logical queue within the shared memory space. A dedicated multicast output port is used to serve multicast cells in a first-in-first-out (FIFO) fashion every cycle. In a given In a given write cycle, upto N

multicast cells or some combination of unicast and multicast cells can be written to the shared memory for switching purposes. During a given read cycle, upto N unicast cells and one multicast can be read out of the shared memory. If a multicast cell is read out of the shared memory, it is routed to the high-speed bus for its replication and transmission to its fanout destinations.

Advantages of SWSR:

Since no replication of a multicast cell takes place before its storage, it is an efficient scheme in terms of memory space. Since no multiple memory accesses are performed for the same information, it is an efficient scheme in terms of the memory access time. In this scheme, sequential read operations are not involved in reading the fanouts of a multicast cell; hence, it is well suited for high-performance shared memory ATM architectures.

Disadvantages of SWSR:

Some additional hardware, such as a fanout bus and an additional buffer or mask at the output ports, is used to perform reading the fanout of a multicast cell within a fixed switching time slot. Use of additional hardware is the only disadvantage of this scheme.

SWSR with Output Buffer (SWSR-OB)

Under this scheme, additional buffers are employed at the output Fig.[3]. The amount of buffer used at the output will depend on the percentage of incoming multicast traffic, the degree average fanouts, and the degree of cell loss rate tolerated by the system. Use of dedicated buffers at the output could also result in excessive cell loss under a bursty traffic consisting of a mix of unicast and multicast cell bursts.

SWSR with Output Mask (SWSR-OM)

This scheme uses a mask called the output mask (OM) to drop additional ATM cells at the output and retain them in the shared memory Fig [4]. In the case of multiple arrivals (i.e. arrival of a unicast cell and a multicast fanout) and depending on the switching priority used, unicast cells or multicast cells are dropped by the output mask (OM) at the output.

This scheme prevents loss of cells at the output ports by retaining the cells (those dropped by the output mask) in the shared memory space and outputting them in the successive switch cycles.

Multicast Cell Enable Block

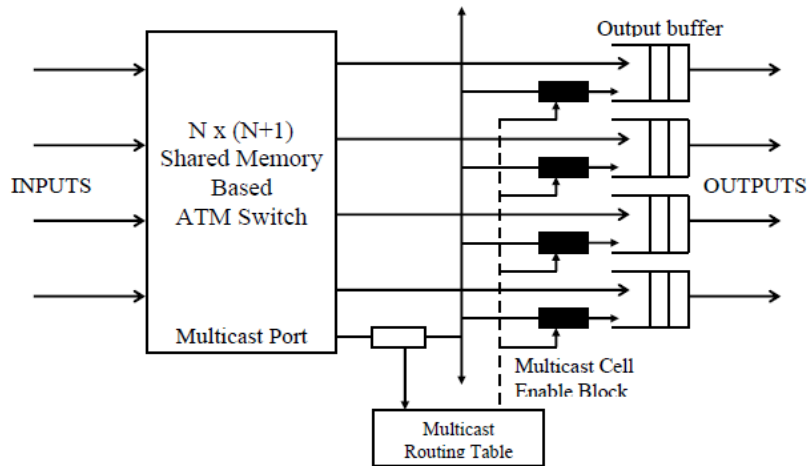


Fig. [3] Shared Memory : Multicasting With Additional Buffer

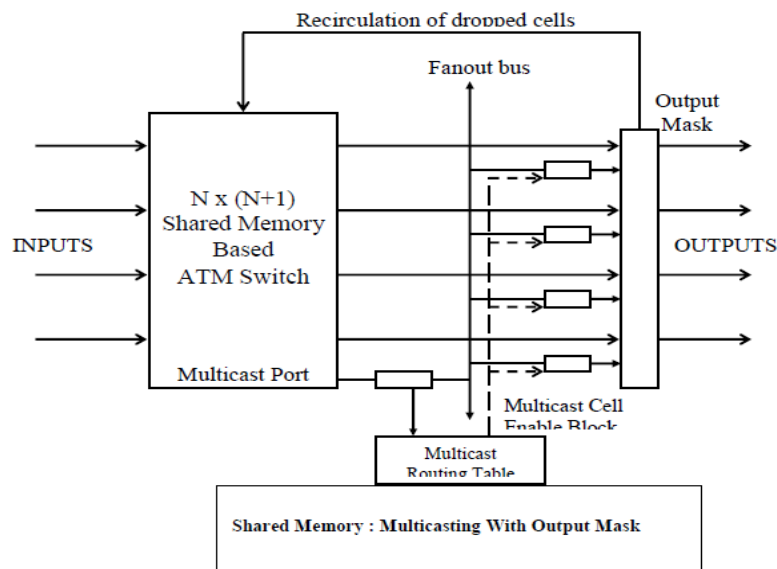


Figure 4: shared Memory Multicasting with Output Mask

6. CONCLUSIONS

Shared memory ATM switches have gained significant importance in handling bursty traffic in ATM networks because of their superior performance characteristics in terms of cell loss and throughput for a given memory space. A shared-memory ATM switch provides sharing of memory space among its switch ports and superior cell loss rate performance compared to input-buffer-based and output-buffer-based ATM switches under condition of identical memory size.

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